REMARKS

This Amendment is in response to the Office Action mailed February 6, 2004. In the Office Action, (i) claims 15-17 were objected/rejected under 35 U.S.C. § 112, 2nd Para.; (ii) claims 1-19 were rejected under 35 U.S.C. § 103(a); and (iii) claims 20-21 were allowable but objected for being dependent. Reexamination and reconsideration in view of the amendments and the remarks made herein is respectfully requested.

Applicant has amended claims 1, 7-8, and 13-20 by this response. Applicant has added new dependent claims 22-41. Accordingly, claims 1-41 are now pending. Of those pending, claims 1, 10, 19, and 20 are independent claims.

Applicant believes that no new matter has been added by this response

I) CLAIM OBJECTIONS - DEPENDENCY

In section 5 of the Office Action, claims 20-21 were indicated as being allowable but objected for being dependent upon a rejected base claim. The Office Action indicated therein that the claims would be allowable if rewritten into independent form including all the limitations of the base claim and any intervening claims. [Office Action, page 12]

Applicant has amended claim 20 into independent form including limitations from the rejected base claim, independent claim 19. There is no intervening claim. Dependent claim 21 now directly depends from an independent claim, claim 20.

Applicant believes the amendment to claim 20 places claims 20-21 in condition for allowance such that this objection is now

moot. Applicant respectfully requests the withdrawal of this objection to claims 20-21.

II) CLAIM REJECTIONS/OBJECTIONS - 35 USC 112, 2nd Paragraph

In section 5 of the Office Action, claims 15-17 were rejected under 35 USC §112, second paragraph as being indefinite. In section 3 of the Office Action, claims 15-17 were objected for the same reason. [Office Action, page 2].

The Office Action particularly pointed to the limitation of "the circuitry" as lacking antecedent basis in the claims.

Applicant has amended the instances of the phrase "the circuitry" to --circuitry-- by deleting the word "the" from the phrase in each claim.

Applicant believes that this amendment to the claims 15-17 now makes this objection and rejection moot and respectfully requests the withdrawal of this claim objection and rejection.

III) Claim Rejections Under 35 U.S.C. § 103(a)

In section 8 of the Office Action, claims 1-9 and 13-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,216,235 issued to Thomas, et al. ("Thomas") in view of U.S. Patent 5,822,596 issued to Casal, et al. ("Casal"). [Office Action, page 3]. Applicant respectfully traverses this rejection.

In section 18 of the Office Action, claims 10-12 and 15-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Thomas. [Office Action, page 7]. Applicant respectfully traverses this rejection.

"To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion of motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)" [MPEP § 2142; 8th Edition, Rev. 1, Feb. 2003, Pg. 2100-124].

Applicant has amended independent claims 1, 10, and 19 to clarify the claimed invention.

Regarding independent claim 1, the Office Action alleges that Thomas teaches "a method comprising: a. determining if a predetermined limit of global functional activity (temperature due to activity) in an integrated circuit has been met or exceeded (temperature has become dangerously high) [col. 3 lines 21-30]; b. and if so, then: i. reducing a high frequency (FMAX) of clocking of circuitry gradually to zero (the minimum frequency may be zero) to stop the clocking of circuitry [col. 3 line 52 through col. 4 line 22 and figure 2]; Thomas teaches detecting the temperature as a global functional activity. Thomas then teaches that if the temperature is met or exceeded the frequency of operation of clocking circuitry is then gradually reduced (including if necessary to a zero frequency)." [Office Action, page 3, lines 8-18]. Applicant respectfully disagrees.

Applicant respectfully submits that Thomas does not disclose "generating a measure of global functional activity in an integrated circuit" and "determining if a predetermined limit of global functional activity in the integrated circuit has been met or exceeded" as recited in amended independent claim 1.

As discussed in Applicant's specification, "[t]he thermal activity detector 310 of the controlled clock generator 202 receives activity information from all of the functional blocks 205, 207, and 209 over activity information signal lines 311 to generate a total measure of functional activity for the integrated circuit 201." "[T]he activity detector 310 monitors the magnitude of the activity of each functional block and adjusts or appropriately weights the level of functional activity of each functional block in order to obtain a measure of global activity to estimate the power consumption and heat generated in the entire integrated circuit. The thermal activity detector 310 determines whether or not the measure of total activity of the integrated circuit meets or exceeds a predetermined limit of activity (referred to as a "thermal limit") where it is desirable to reduce the heat generated by the activity in the integrated circuit to achieve a safe temperature level." [Specification, page 8, lines 22-26 and page 8, line 32 through page 9, line 10].

Applicant's measure of global functional activity is not disclosed by Thomas's temperature sensor 4. Thomas's "temperature sensor 4 is either integrated within the Very Large Scale Integration (VLSI) design of the microprocessor 2 or placed in contact with the housing or package thereof. In either case, the temperature sensor 4 is thermally coupled with the microprocessor 2. ... The temperature sensor 4 produces a temperature signal 6." [Thomas, Col. 3, lines 41-51].

Thomas's temperature sensor 4 does not receive activity levels from functional blocks within an integrated circuit and generate a measure of global functional activity there from. Moreover, Thomas's temperature sensor 4 may be heated from other heat generating sources within an integrated circuit. For example, if the output drivers of an integrated circuit drive high currents into a large load, the integrated circuit can heat up regardless of the activity level in the functional blocks. Furthermore due to thermal resistances, such as from the package or IC substrate, there is a time delay in the generation of any temperature signal by Thomas's temperature sensor 4 from any heat that is generated. Thus, Thomas's temperature sensor 4 does not generate a measure of global functional activity as does Applicant's claimed invention.

Moreover, Thomas does not disclose a predetermined limit of global functional activity. Thomas's "fast clock" is not regulated in response to functional activity but temperature. Thomas's "fast clock is [a clock signal having a] temperature regulated maximum frequency". [Thomas, Col. 4, lines 62-64]. Thomas's disclosure of a threshold temperature for a chip beyond which a maximum frequency is limited, does not disclose a predetermined limit of global functionality. [Thomas, col. 4, lines 8-11].

Nor does Casal disclose "generating a measure of global functional activity in an integrated circuit" and "determining if a predetermined limit of global functional activity in the integrated circuit has been met or exceeded" as recited in amended independent claim 1. Casal is triggered upon a system power up or a system power down without concern of functional activity within an integrated circuit.

Additionally, the Office Action admits that "Thomas does not expressly disclose waiting a predetermined time period after stopping the clocking of circuitry and starting the clocking of circuitry at a low frequency". [Office Action, page 3, lines 19-20].

However, the Office Action alleges that "Casal teaches waiting a predetermine time (sufficient stabilization time) after stopping (powering down) the clocking of circuitry (for logic circuits) and starting the clocking circuitry at a low frequency [col. 1 line 56-61, col. 1 line 56 through col. 1 line 4 and col. 3 line 58 through col. 4 line 11]." [Office Action, page 3, lines 21-24]. Applicant respectfully disagrees.

Casal only discloses that "the frequency of the clock signal should be increased/decreased in steps with sufficient time at intermediate frequencies to allow stabilization until power up/power down is complete." [Casal, Col. 1, lines 44-47]. Casal does not disclose waiting any period of time after power down is complete and then powering up. Applicant respectfully submits that Casal does not disclose "waiting a predetermined time period after stopping the clocking of circuitry and starting the clocking of circuitry at a low frequency" as recited in independent claim 1.

Thus, Applicant respectfully submits that Thomas and Casal, alone or in combination, do not make obvious Applicant's claimed invention of independent claim 1.

Dependent claims 2-9 depend from independent claim 1. Applicant believes that it has placed claim 1 in condition for allowance such that claims 2-9 depending there from with additional limitations are also in condition for allowance.

Regarding independent claim 10, the Office Action alleges that "Thomas teaches a circuit comprising: a. a clock generator

(oscillator 8, 22,52 and clock input of different embodiments) to generate a clock [figures 1,3,4,5,9 and 10]; b. an activity detector (activity detector) to measure global functional activity of the circuit and temperature sensor (temperature due to processor activity) [figures 3, 5,7,9, and 10; col. 4 lines 30 et seq.]; c. a clock throttling controller (clock regulation unit 20) coupled to the activity detector and the clock generator, the clock throttling controller to generate a throttled clock to couple to functional blocks (i/o ports, instruction cache, current instruction, program counter) of the circuit for clocking circuitry therein, the clock throttling controller to gradually throttle the frequency of the throttled clock to the functional blocks in response to the measure of the global functional activity meeting (reaching a lower) or exceeding (falling below a lower limit) a predetermined limit [col. 5 line 38 through col. 6 line 9]. [Office Action, page 7, line 11 through page 8, line 2]. Applicant respectfully disagrees.

The Office Action goes further to say that "Thomas also teaches the case wherein the temperature causes the clock to be throttled in response to activity. If the activity were very high for a sustained period of time the temperature would reach above a predetermined threshold causing throttling to take place [col. 4 lines 1-22]. [Office Action, page 8, lines 3-5]. Applicant respectfully disagrees.

Thomas's activity detector 12 does not measure global functional activity of an integrated circuit. Thomas's activity detector 12 only monitors a system to provide an indication as to whether or not Thomas's microprocessor 2 has some processing to do or not, so that it can be put to sleep. If Thomas's activity detector 12 determines there is some processing to

perform, "the activity detector 12 notifies the VCO controller 16 that processing is needed with the activity signal 14. On the other hand, when no activity exists, the activity detector 12 notifies the VCO controller 16 that no processing is needed with the activity signal 14." [Thomas, Col. 4, lines 35-39]. "[I]f the activity detector 12 indicates that no processing is needed at a given point in time, then regardless of the temperature detected by the temperature sensor 4, the VCO controller 16 will cause the VCO 8 to produce a sleep (or slow) clock." [Thomas, Col. 4, lines 54-58].

Thomas's activity detector 12 does not receive levels of activity from functional blocks of the integrated circuit to be capable of measuring the global functional activity therein. Thomas's activity detector 12 externally "monitors the microprocessor 2 and/or some related peripheral device (e.g., interrupt controller, keyboard buffer, input/output ports, instruction cache, current instruction, program counter)" as is illustrated in Figure 3. Even if integrated with the microprocessor, Thomas's "activity detector 48 [functions] similarly to the activity detector 12" and receives external types of activity inputs such as "an interrupt, keyboard activity, modem line activity, I/O port activity, or processor activity" to indicate whether or not the type of activity exists at all. [Thomas, Col. 6, lines 53-55, 57-61]. That is, Thomas's activity detectors do not receive levels of activity from functional blocks of an integrated circuit. Moreover, the output from Thomas's activity detectors, "the activity signal is a digital signal which is "high" or "1", when activity is present and "low" or "0" when no activity is present." [Thomas, Col. 5, lines 58-60]. Thomas's activity signal indicates when

no activity is present and does not provide a measure of global functional activity within an integrated circuit.

Thus, Applicant respectfully submits that Thomas does not disclose "an activity detector to measure global functional activity of the integrated circuit" as recited in independent claim 10. [Claim 10, lines 3-4].

Additionally, the Office Action alleges that Thomas's clock regulation unit 20 discloses Applicant's clock throttling controller to which Applicant respectfully disagrees. Thomas's clock regulation unit 20 does not ***gradually*** throttle a frequency of a clock. Thomas's logic gates 26,28,32,34,36,and 38 of Thomas's clock regulation unit 20 "operate to select either the fast clock or the sleep clock". [Thomas, Col. 5, lines 64-65]. Thomas's clock regulation unit 20 doesn't gradually step down the clock frequency or gradually step up the clock frequency but switches between two frequencies, a fast clock or a sleep clock.

Furthermore, Applicant respectfully submits that Thomas does not disclose generating a throttled clock in response to the measure of the global functional activity of an integrated circuit. Contrary to the allegations of the Office Action, Thomas's temperature sensor 4 does not measure the global activity within an integrated circuit. As discussed previously, Thomas's temperature sensor 4 does not receive activity levels from functional blocks within an integrated circuit and generate a measure of global functional activity there from. Moreover, Thomas's temperature sensor 4 may be heated from other heat generating sources within an integrated circuit. For example, if the output drivers of an integrated circuit drive high currents into a large load, the integrated circuit can heat up regardless of the activity level in the functional blocks. Furthermore due to thermal resistances, such as from the package

or IC substrate, there is a time delay in the generation of any temperature signal by Thomas's temperature sensor 4 from any heat that is generated. Thomas's temperature sensor 4 does not generate a measure of global functional activity as does Applicant's claimed invention. Thus, Thomas's clock regulation unit 20 is not responsive to global functional activity within an integrated circuit, regardless of whether or not a predetermined limit is met or exceeded.

Thus, Applicant respectfully submits that Thomas does not disclose a "clock throttling controller to generate a throttled clock to couple to functional blocks of the integrated circuit for clocking circuitry therein, the clock throttling controller to gradually throttle the frequency of the throttled clock to the functional blocks in response to the measure of the global functional activity meeting or exceeding a predetermined limit" as recited in independent claim 10. [Claim 10, lines 6-13].

For the foregoing reasons, Applicant respectfully submits that Thomas does not make obvious Applicant's claim 10.

Regarding dependent claims 11-12, the Office Action alleges that "Thomas further [teaches], at col. 4 lines 30-35, wherein the activity detector receives measures of local functional activity associated with each functional block of the integrated circuit to measure the global functional activity of the integrated circuit. Wherein interrupt controllers, input/output ports, instruction cache, current instruction, and program counter are interpreted to be functional blocks of the integrated circuit." [Office Action, page 8, lines 16-20]. Applicant respectfully disagrees.

Thomas's activity detector 12, described in Thomas's col. 4, lines 30-35 as cited by the Office Action, is illustrated in Figure 3 as being external to Thomas's microprocessor 2. Thus

it stands to reason that Thomas's "related peripheral device (e.g., interrupt controller, keyboard buffer, input/output ports, instruction cache, current instruction, program counter)" are being monitored externally from Thomas's microprocessor 2 and are thus not functional blocks thereof.

The Office Action further alleges that "Thomas uses the activity of different functional blocks to make a determination as to the global activity of the microprocessor." [Office Action, page 8, line 20 through page 9, line 2]. Applicant respectfully disagrees.

As previously discussed, Thomas's related peripheral devices are not functional blocks of Thomas's microprocessor. Additionally the output from Thomas's activity detectors, "the activity signal is a digital signal which is "high" or "1", when activity is present and "low" or "0" when no activity is present." [Thomas, Col. 5, lines 58-60]. Thomas's activity signal that indicates when no activity is present, does not provide a measure of global functional activity within an integrated circuit.

Regarding dependent claims 14-17, Thomas only discloses controlling a global clock to Thomas's microprocessor 2 and not a local clock to a functional block. Moreover, Thomas does not disclose selectively clocking circuitry within a functional block.

Regarding dependent claim 18, Applicant has amended claim 18 to clarify that "the frequency of the throttled clock is gradually throttled OFF in response to the measure of the functional activity meeting or exceeding the predetermined limit."

With respect to dependent claim 18, the Office Action alleges that "Thomas further [teaches] wherein, the frequency of

the throttled clock is gradually throttled in response to the measure of the functional activity meeting or exceeding the predetermined limit [col. 4 lines 46-64]." [Office Action, page 11, lines 13-15]. Applicant respectfully disagrees.

As discussed previously, Thomas's temperature sensor 4 does not generate a measure of global functional activity but a temperature signal 6. Nor does Thomas's activity detector 12 generate a measure of global functional activity but an "activity signal [that] is a digital signal which is "high" or "1", when activity is present and "low" or "0" when no activity is present." [Thomas, Col. 5, lines 59-61].

Thomas's activity signal causes Thomas's VCO 8 to switch between a fast clock and a slow clock. "[I]f the activity detector 12 indicates that no processing is needed at a given point in time, then regardless of the temperature detected by the temperature sensor 4, the VCO controller 16 will cause the VCO 8 to produce a sleep (or slow) clock." [Thomas, Col. 4, lines 54-58]. "On the other hand, if the activity detector 12 indicates that processing is needed at this point in time, then the VCO controller 16 will cause the VCO 8 to produce a fast clock." [Thomas, Col. 4, lines 59-62]. There is no gradual throttling down or up of any clock when Thomas switches between a fast clock and a slow clock in response to Thomas's activity signal.

As discussed previously, Thomas does not disclose a predetermined limit of global functional activity. Thomas's "fast clock" is not regulated in response to functional activity but temperature. Thomas's "fast clock is [a clock signal having a] temperature regulated maximum frequency". [Thomas, Col. 4, lines 62-64]. Thomas's disclosure of a threshold temperature for a chip beyond which a maximum frequency is limited, does not

disclose a predetermined limit of global functionality. [Thomas, col. 4, lines 8-11].

Additionally, the Office Action takes Official Notice here and elsewhere (e.g., claim 15) that systems with sleep clocks have zero frequency. Applicant respectfully challenges the taking of official notice as a free running clock would not have zero frequency, it wouldn't exist as it's a DC signal. Thomas switches between a free running fast clock and a free running sleep clock that is synchronized with the fast clock through a divider. Thomas does not disclose control logic to synchronize switching between a zero frequency signal and a fast clock.

Regarding dependent claims 13-14, Applicant has amended dependent claims 13-14 to clarify the claimed invention.

In the Office Action with respect to claims 13 and 14, it is alleged that "Thomas teaches gradually throttling the clock using a control signal based on activity to control the frequency of an oscillator". [Office Action, page 9, lines 14-16]. Applicant respectfully disagrees for the reasons set forth elsewhere herein.

The Office Action further alleges that Casal discloses a "logical gate to periodically mask out one or more clock cycles of the clock (at 110) to generate the throttled clock in response to the control signal to gradually throttle the frequency of the throttled clock" and that "Casal uses a clocked RS flip-flop (208) [to] periodically masks out one or more clock cycles." [Office Action, page 9, lines 19-21 and page 10, lines 1-2]. Applicant respectfully disagrees.

Casal does not disclose masking out clock cycles to throttle a clock up and down. As admitted in the Office Action, Casal uses frequency dividers to decrease the clock frequency and not masked out clock cycles. Casal only discloses Casal's

"divider 104 receives a clock signal from system clock 101, divides the frequency of the clock signal by some number according to a two-bit input." [Casal, col. 4, lines 18-21]. Casal's clocked set reset flip flop 208 is part of Casal's divider 104.

Moreover, Casal's clocked set reset flip flop 208 does not mask out transitions in Casal's clock input at 208. Casal's clock input at 208 only synchronizes transitions of the set and reset inputs from blocks 204 and 203, respectively. That is, Casal's clocked set reset flip flop 208 and any logical gate therein does not disclose a "logical gate to periodically mask out one or more clock cycles of the clock to generate the throttled clock in response to the control signal" as recited in Applicant's amended claims 13-14.

Moreover, dependent claims 11-18 depend from independent claim 10. Applicant believes that it has placed independent claim 10 in condition for allowance such that claims 11-18 depending there from with additional limitations are also in condition for allowance.

Regarding independent claim 19, Applicant has amended claim 19 in order to clarify the claimed invention.

With regards to independent claim 19, the Office Action alleges that because "Thomas taught the claimed integrated circuit therefore he also taught the claimed clock generator." [Office Action, page 12, lines 3-4]. Applicant respectfully disagrees.

As discussed previously with respect to independent claim 10, Thomas does not disclose Applicant's claimed activity detector and does not disclose Applicant's claimed clock throttling controller. The detailed remarks with respect to independent claim 10 are incorporated here by reference.

Applicant respectfully submits that Thomas does not make obvious the elements of independent claim 19.

In conclusion, Applicant respectfully requests the withdrawal of the 35 USC 103(a) claim rejections of claims 1-19 for the foregoing reasons.

IV) NEW CLAIMS

Applicant has added new dependent claims 22-41.

New claims 22-26, 27-34, and 35-41 respectively depend directly or indirectly from independent claims 1, 10, and 19.

Applicant respectfully submits that the temperature levels recited in the claims are well known and are supported by the prior art references submitted herewith in an information disclosure statement.

Applicant believes that it has placed independent claims 1, 10, and 19 in condition for allowance such that dependent claims depending there from with further limitations are also in condition for allowance. Applicant respectfully submits that new claims 22-41 are also in condition for allowance.

V) CLAIM AMENDMENTS

Applicant has amended claims 1, 7-8, and 13-20.

As discussed previously, claim 20 was amended into independent form, claims 1, 10, 13-14, and 18-19 were amended to clarify the invention unrelated to reasons of patentability, and claims 15-17 were amended to overcome a claim objection. Claims 7-8 were also amended to clarify the claimed invention for reasons unrelated to patentability.

CONCLUSION

In view of the foregoing it is respectfully submitted that the pending claims are in condition for allowance.

Reconsideration of the rejections and objections is requested. Allowance of the claims at an early date is solicited.

The Examiner is invited to contact Applicant's undersigned counsel by telephone at (714) 557-3800 to expedite the prosecution of this case should there be any unresolved matters remaining.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such deposit account.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: July 12, 2004

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